AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and indicates the status of the claim in parenthesis. Additions are indicated by underlining, deletions by strikethrough.

Listing of Claims

1. (Currently Amended) A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region; ~~and~~

a plurality of bonding pads disposed on only one side of the semiconductor chip on the peripheral circuit region; and

a plurality of leads formed on a side of the semiconductor chip opposite the side on which the bonding pads are disposed for connection with the bonding pads.

2. (Original) The device of claim 1, wherein the plurality of bonding pads are disposed in at least one row.

3. (Original) The device of claim 2, wherein the plurality of bonding pads are disposed in two rows.

4. (Canceled)

5. (Currently Amended) The device of claim 41, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads, respectively, with a portion of the bonding pads so as to cross the memory cell array region.

6-7 (Canceled)

8. (Currently Amended) A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region;

a plurality of bonding pads disposed in at least one row on only one side of the semiconductor chip on the peripheral circuit region;) ~~The device of claim 2, further comprising~~:

a first leads group disposed adjacent to the bonding pad side of the semiconductor chip;

a second leads group disposed opposite the first leads group; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads.

9. (Original) The device of claim 8, wherein the second leads group disposed opposite the first leads group are located to a side of the semiconductor chip opposite the bonding pad side.

10. (Original) The device of claim 8, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being disposed over the peripheral circuit region, the second plurality of bonding wires being disposed over the memory cell array region.

11. (Original) The device of claim 8, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and the second row of bonding pads being

electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region.

12. (Original) The device of claim 8, wherein the second leads group extends over a portion of the semiconductor chip region.

13. (Original) The device of claim 12, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being disposed over the peripheral circuit region, the second plurality of bonding wires being disposed over the memory cell array region.

14. (Original) The device of claim 12, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and a second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region.

15. (New) A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region;

a plurality of bonding pads disposed on only one side of the semiconductor chip; and

a plurality of leads formed on a side of the semiconductor chip opposite the one side on which the bonding pads are disposed for connection with the bonding pads.

16. (New) The device of claim 15, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads to corresponding bonding pads disposed on the one side so as to cross the memory cell array region.

17. (New) The device of claim 15, wherein the plurality of bonding pads are disposed in at least one row.

18. (New) The device of claim 17, wherein the plurality of bonding pads are disposed in two rows.

19. (New) The device of claim 15, wherein

the semiconductor chip includes a peripheral circuit region surrounding the memory cell array region, and

the bonding pads are disposed on the one side of the semiconductor chip on the peripheral circuit region.